What is claimed is:

[Claim 1] A method for improving hot carrier effects in complementary metal oxide semiconductor (CMOS) devices, the method comprising:

forming a first configuration of insulating material over a first group of the CMOS devices; and
forming a second configuration of insulating material over a second group of the CMOS devices;
wherein said first and said second configurations of insulating material are formed subsequent to a silicidation of the CMOS devices and prior to formation of a first interlevel (ILD) dielectric material over the CMOS devices.

[Claim 2] The method of claim 1, wherein said first configuration further comprises at least a pair of individual insulating layers, and said second configuration of insulating devices further comprises a single insulating layer.

[Claim 3] The method of claim 2, wherein said first group of the CMOS devices comprises NFET devices and said second group of the CMOS devices comprises PFET devices.

[Claim 4] The method of claim 2, wherein said first group of the CMOS devices comprises gate oxide thicknesses of a first range and said second group of the CMOS devices comprises gate oxide thicknesses of a second range.

[Claim 5] The method of claim 2, wherein said pair of individual insulating layers further comprises a first nitride layer and an oxide layer, and said single insulating layer further comprises a second nitride layer.

[Claim 6] The method of claim 5, wherein said first nitride layer is a tensile nitride layer, and said second nitride layer is a compressive nitride layer.

[Claim 7] The method of claim 6, wherein said first nitride layer is Si_3N_4 deposited using a BTBAS (Bis(TertiaryButylAmino)Silane) precursor, said second nitride layer is Si_3N_4 deposited by plasma enhanced chemical vapor deposition

(PECVD) using a silane (SiH_2) precursor, and said oxide layer is tetraethyl orthosilicate (TEOS).

[Claim 8] The method of claim 2, wherein said pair of individual insulating layers further comprises a first nitride layer and a third nitride layer, and said single insulating layer further comprises a second nitride layer.

[Claim 9] The method of claim 2, wherein said pair of individual insulating layers further comprises a first nitride layer and an oxide layer, and said single insulating layer further comprises said first nitride layer.

[Claim 10] The method of claim 2, wherein said pair of individual insulating layers further comprises a first nitride layer and a second nitride layer, and said single insulating layer further comprises said first nitride layer.

[Claim 11] The method of claim 1, wherein:

said first configuration of insulating material further comprises one of a single nitride layer and a single oxide layer; and
said second configuration of insulating material further comprises one of a single nitride layer, a single oxide layer, and a combination of a nitride and an oxide layer.

[Claim 12] The method of claim 1, wherein said first configuration of insulating material comprises a compressive material and said second configuration of insulating material comprises a tensile material.

[Claim 13] A structure for improving hot carrier effects in complementary metal oxide semiconductor (CMOS) devices, comprising:

a first configuration of insulating material formed over a first group of the CMOS devices; and
a second configuration of insulating material formed over a second group of the CMOS devices;
wherein said first and said second configurations of insulating material are formed subsequent to a silicidation of the CMOS devices and prior to formation of a first interlevel (ILD) dielectric material over the CMOS devices.

[Claim 14] The structure of claim 13, wherein said first configuration further comprises at least a pair of individual insulating layers, and said second configuration of insulating devices further comprises a single insulating layer.

[Claim 15] The structure of claim 14, wherein said first group of the CMOS devices comprises NFET devices and said second group of the CMOS devices comprises PFET devices.

[Claim 16] The structure of claim 14, wherein said first group of the CMOS devices comprises gate oxide thicknesses of a first range and said second group of the CMOS devices comprises gate oxide thicknesses of a second range.

[Claim 17] The structure of claim 14, wherein said pair of individual insulating layers further comprises a first nitride layer and an oxide layer, and said single insulating layer further comprises a second nitride layer.

[Claim 18] The structure of claim 17, wherein said first nitride layer is a tensile nitride layer, and said second nitride layer is a compressive nitride layer.

[Claim 19] The structure of claim 18, wherein said first nitride layer is Si_3N_4 deposited using a BTBAS (Bis(TertiaryButylAmino)Silane) precursor, said second nitride layer is Si_3N_4 deposited by plasma enhanced chemical vapor deposition (PECVD) using a silane (SiH_2) precursor, and said oxide layer is tetraethyl orthosilicate (TEOS).

[Claim 20] The structure of claim 14, wherein said pair of individual insulating layers further comprises a first nitride layer and a third nitride layer, and said single insulating layer further comprises a second nitride layer.

[Claim 21] The structure of claim 14, wherein said pair of individual insulating layers further comprises a first nitride layer and an oxide layer, and said single insulating layer further comprises said first nitride layer.

[Claim 22] The structure of claim 13, wherein said pair of individual insulating layers further comprises a first nitride layer and a second nitride layer, and said single insulating layer further comprises said first nitride layer.

[Claim 23] The structure of claim 13, wherein:

said first configuration of insulating material further comprises one of a single nitride layer and a single oxide layer; and
said second configuration of insulating material further comprises one of a single nitride layer, a single oxide layer, and a combination of a nitride and an oxide layer.

[Claim 24] The structure of claim 13, wherein said first configuration of insulating material comprises a compressive material and said second configuration of insulating material comprises a tensile material.